Listing of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A system, comprising:

a first processor;

a second processor coupled to the first processor, the second processor having a core and comprising stack storage residing in the core;

memory coupled to, and shared by, the first and second processors; and

a synchronization unit coupled to the first and second processors, said synchronization unit synchronizes the execution of the first and second processors;

wherein the second processor executes stack-based instructions while the first processor executes one or more tasks wherein the first processor manages the memory via an operating system that executes only on the first processor and the first processor executes a virtual machine that controls the execution of a program on the second processor;

wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode; and

wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor.

2. (Original) The system of claim 1 wherein the second processor comprises an internal data memory that holds a contiguous block of memory defined by an address stored in a register, and wherein local variables are stored in said data memory.

3. – 4. (Cancelled).

5. (Original) The system of claim 1 wherein the stack-based instructions comprise Java

bytecodes and the first processor comprises a RISC processor so that the RISC processor executes one or more tasks while the second processor executes Java code.

6. (Original) The system of claim 1 further including a main stack residing outside the second processor's core and coupled to the stack storage in the second processor's core.

7. (Original) The system of claim 6 wherein the stack storage in the second processor's core provides an operand to execute a stack-based instruction in the second processor.

8.-9. (Canceled)

10. (Previously Presented) A method, comprising:

synchronizing the execution of first and second processors, the second processor having a core and comprising stack storage residing in the core, wherein synchronizing comprises detecting that the first processor is executing a transaction targeting a pre-determined address and asserting a wait signal to cause said first processor to enter a reduced power or reduced performance mode and synchronizing further comprises the second processor causing the wait signal to be de-asserted to terminate the first processor's reduced power or reduced performance mode;

executing stack-based instructions in the second processor while the first processor executes one or more tasks;

executing an operating system on the first processor and not on the second processor;

executing a virtual machine on the first processor that controls the execution of a program on the second processor; and

the first processor managing memory accessible to both the first and second processors via the operating system.

11. (Original) The method of claim 10 further including storing local variables in an internal data memory in the second processor, the internal data memory configured to store a contiguous block of memory defined by an address stored in a register.

12. – 13. (Cancelled).

14. (Original) The method of claim 11 further comprising providing a main stack residing outside the second processor's core and providing an operand from the stack storage in the second processor's core and executing a stack-based instruction in the second processor using the operand.

15.-16. (Canceled)

17. (Previously Presented) A system, comprising:

a first processor;

a second processor coupled to the first processor, the second processor having a core and comprising stack storage residing in the core and having an internal data memory that holds a contiguous block of memory defined by an address stored in a register, and wherein local variables are stored in said data memory;

memory coupled to, and shared by, the first and second processors; and

a synchronization unit coupled to the first and second processors, said synchronization unit asserts a first signal to the first processor to cause the first processor to cease executing instructions and said synchronization unit receives a second signal from the second processor which thereby causes the synchronization unit to de-assert the first signal;

wherein the second processor executes stack-based instructions while the first processor executes one or more tasks wherein the first processor manages the memory via an operating system that executes only on the first processor and the first processor executes a virtual machine that controls the execution of a program on the second processor.

18. – 19. (Cancelled).

20. (Previously presented) The system of claim 1 wherein a clock internal to the first processor is disabled thereby effectuating the reduced power or reduced performance mode.

21. (Previously Presented) The system of claim 1 wherein said wait signal remains asserted until said synchronization unit deasserts said wait signal.

22. (Previously Presented) The system of claim 1 wherein said second processor asserts said wait release signal when said second processor requires support from said first processor.

23. (Previously Presented) The system of claim 17 wherein said synchronization unit continues to assert said first signal until the synchronization unit either the synchronization unit receives said second signal from the second processor or the synchronization unit receives an interrupt signal.

24. (Previously Presented) The system of claim 17 wherein said second processor asserts said second signal when said second processor requires support from said first processor.